A Very Fast and Low Power Incrementer and Decrementer Circuit

Samiappa Sakthikumaran[1], S. Salivahanan, V. S. Kanchana Bhaaskaran[2], V. Kavinilavu
B. Brindha and C. Vinoth
SSN College of Engineering, Kalavakkam, Rajiv Gandhi Salai, (Off) Chennai, Tamil Nadu, India
Email: vskanchana@hotmail.com

***Abstract*— An Incrementer/Decrementer (INC/DEC) is an important building block in many digital systems such as the address generation unit of microcontrollers and microprocessors. In this paper, we propose novel architectures and designs for very fast and low power INC/DEC circuits that can be used in Low power RISC processors. The designs operate on the 2N-2N2P energy recovery logic design approach. The 350nm technology library files from AMS350nm standard CMOS technology are used in the work.**

***Index Terms*— Adiabatic Logic, low power, 2N-2N2P adiabatic logic, Incrementer, Decrementer**

I. INTRODUCTION

The design of high-speed and low-power VLSI architectures needs efficient processing units, which are optimized for the speed and power consumption. Hence, the trend has been to search for techniques to reduce the power dissipation, low power operation, and designing for energy recovery and recycling. Energy recovery is proving to be a promising approach for the design of low power VLSI circuits. The primary advantage of these circuits results from its inherent characteristics of

- deriving a constant current from the power clock
- get the FETs working with the minimum voltage between the source and drain terminals. The basic complementary function Block of 2N-2N2P is shown in Fig. 1.

The module INC/DEC counts up or counts down during every clock cycle. This building block in widely used in digital systems, such as the program counter [l] and frequency divider [2]. A pre-loadable up/down counter [3] [4] is used as an INC/DEC. However, [3] or [4] incur a speed limitation in the process of generating the carry bit. This is due to the fact that the up/down counter is designed using the concept of conventional addition operation, although [5] uses the half-adder to replace the full-adder. [6] Presents a decrementer architecture employing a data-out multiplexer array and a decision block but the latency remains high due to the generation of select bit.

In this paper, we propose a structure which can realize the *incrementing* and *decrementing* operations, during incrementing/decrementing operations in the arithmetic units, for incrementing the address information of the program counter and for incrementing and decrementing operations of the stack pointer in the processors. The INC/DEC circuit structure realizes reduced delay and power, and enhanced low power dissipation characteristics.

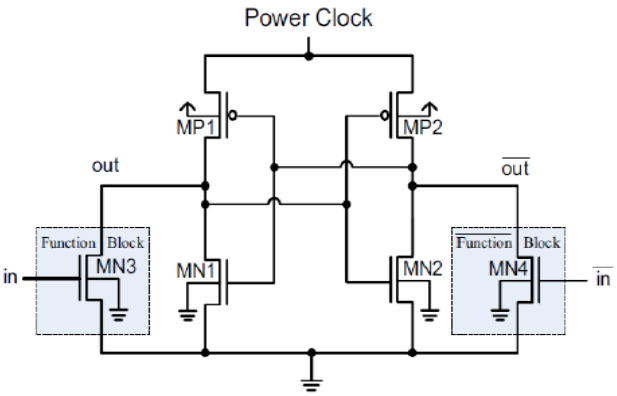

Figure 1 2N-2N2P adiabatic logic.

The rest of this paper is organized as follows. Section II presents a review of the conventional INC/DEC structures. Section III presents the proposed architecture. Section IV depicts the design flow of CMOS and adiabatic INC/DEC design counterparts. The front-end design flow is also discussed in this section. Section V presents the results and analysis. The comparative performance behavior between the proposed architecture and the conventional CMOS circuits is discussed. Section VI concludes.

II. CONVERNTIONAL INCREMENTER CIRCUITS

Figure 2 shows the internal logic circuit schematic of an *incrementer*, based on the conventional 4-bit ripple carry adder. The half adders, denoted by HA, are used for constructing the incrementer structure. Fig. 3 depicts the internal logic diagram of a 4-bit ripple carry *decrementer*. In these designs, the critical delay for the incrementing/decrementing operation is determined by the delay incurred in the carry bit propagation time, through the chain of AND gates. As the size of the chain grows, this delay also increases, making the delay of the most significant bit (MSB), the largest one in the process. In the proposed design, the carry is calculated using parallel AND chain thereby reducing the delay incurred

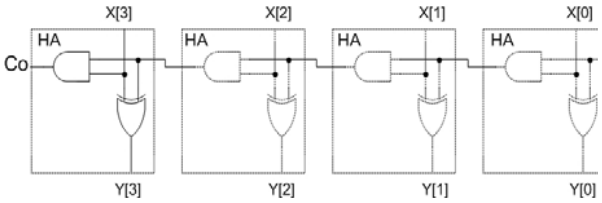

Figure 2. Ripple-Carry Incrementer

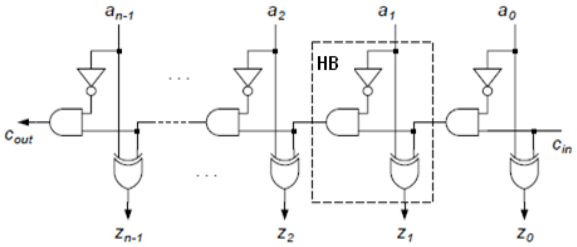

Figure 3. Ripple-carry Decrementer

by MSB. The latency, power dissipation, the combinational path delay and the energy consumed are calculated and compared for these circuits.

III. PROPOSED ARCHITECTURE

The design employs the carry select adder method in place of the conventional ripple-carry adder structure. This speeds up the process of the action of incrementing and decrementing (INC/DEC). The basic schematic block of the proposed carry select incrementer is shown in Fig. 4. It considers the carry_in to be a logic High always. The addition function of the proposed circuit is accomplished by the 4-bit basic block. The incrementing action or the retaining of the current value is achieved by the use of the 2-to-1 multiplexer. This accomplishes fast incrementing action along with a reduced number of function stages, thus reducing the latency of the circuit. The resultant advantage of this basic block is the large silicon area reduction realized, when the INC/DEC is designed for a wider word length of data. To explain the operation of the logic block better, the Boolean expressions depicting the 4-bit basic block are given below:

B1=~A0; B2=A1^A0;
C1=A1*A0; C2=A2*A3;
C0=C1*C2; C3=C1*A2;
B3=A2^C1; B4=A3^C3;

It can be seen that the carry_out bit of the block is calculated in parallel along with B3 by using a parallel chain of AND gates. On the other hand, the RCA structure uses a series pattern of carry propagation. This reduces the delay when compared with the conventional methods of incrementer structures.

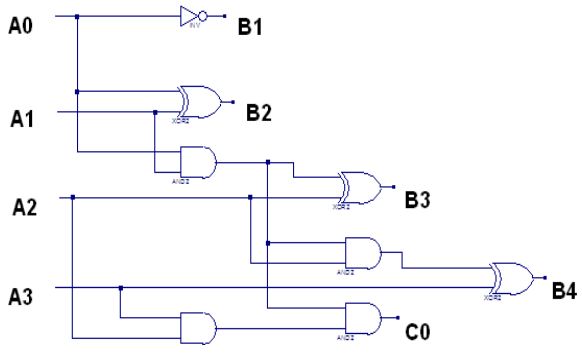

Figure 4. Basic Block of CSI

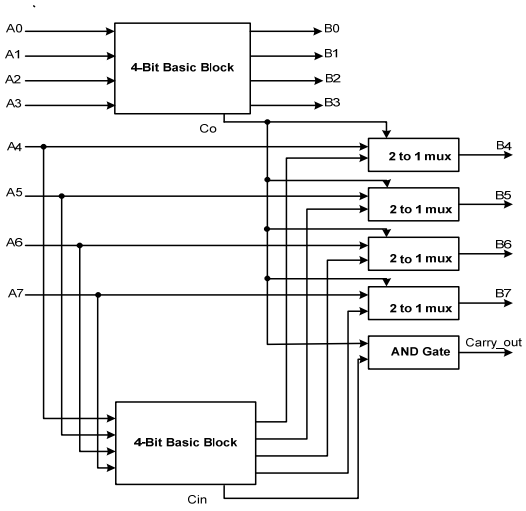

Figure 5 Proposed Incrementer Block Diagram

The block diagram of the INC/DEC is shown in Fig. 5 and Fig. 6 respectively. The incrementer structure divides the word-size equally into blocks of 4-bits each. Each ripple carry block is replaced by the proposed block, which reduces the latency and number of devices utilized when the function is designed with large number of bits. The decrementer structure inherits the fast incrementer structure with inverters in both sides to provide a fast decrementing action, along with gaining the advantages of the incrementer structure.

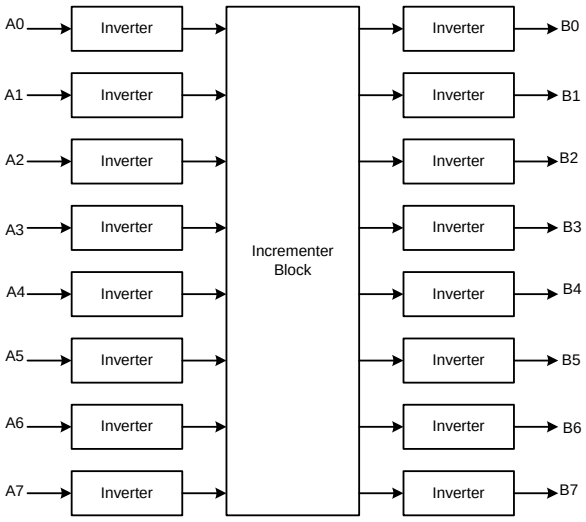

Figure 6. Proposed Decrementer Block Diagram

IV. DESIGN FLOW

A. *FRONT-END DESIGN*

The INC/DEC design has been developed using Verilog-HDL and synthesized using the Synopsys Front-end Design Compiler. The generic libraries of SAED 90nm technology has been used in the designs. The design area and the combinational path delay have been estimated for both the conventional and proposed INC/DEC designs and the results are compared in Tables I and II.

TABLE I
PATH DELAY AND AREA

Circuit Structure	Incrementer		Decrementer	
	Combinational path delay(ns)	Area (um^2)	Combinational path delay(ns)	Area (um^2)
Ripple-carry	16.201	374.01	16.680	352.7
Proposed	12.122	346.5	13.880	331.4

Figure 7. Ripple-carry Incrementer

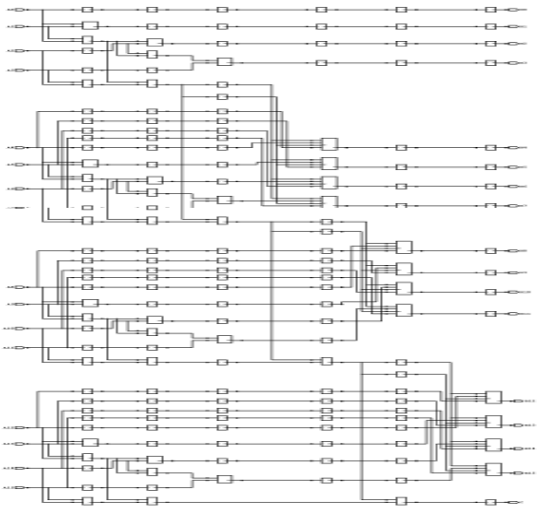

Figure 8. Proposed CMOS-Logic Incrementer Schematic

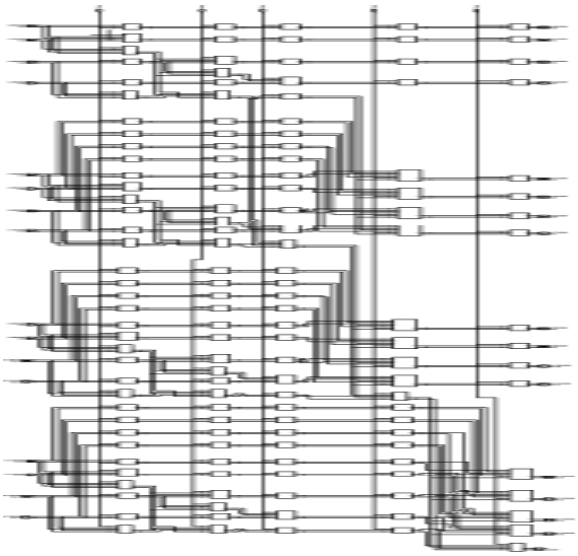

Figure 9. Adiabatic-Logic proposed Incrementer

TABLE II
NO. OF DEVICES (N) AND LATENCY (L) COMPARISON

Circuit Structure	Incrementer		Decrementer	
	N	L	N	L
Ripple-carry	1152	16	1200	16
Proposed CMOS	804	6	868	8
Adiabatic	1040	5	1004	5

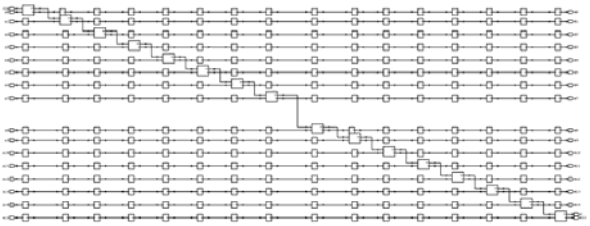

Figure 10. Ripple-carry Decrementer

B. BACK-END DESIGN

The conventional INC/DEC is designed in Tanner EDA using AMS350nm technology from Austria Micro Systems. The design is implemented by using the 2N-2N2P quasi-adiabatic logic style. The design is also implemented using the conventional CMOS logic counterpart for justifiable comparison. Figs. 7 to 12 depict the circuit diagrams. The latency, power dissipation and energy are calculated for each of the circuit design methods.

The latency represents the number of logic stages incurred by the circuit to produce the output in response to the input. The power dissipation measured indicates the average power measured over the simulation time. The simulation is carried out over a wide range of input data values. The results so obtained are tabulated in Tables III and IV.

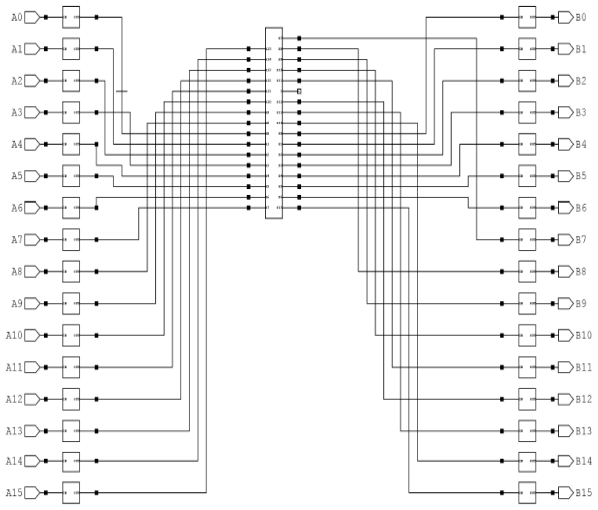

Figure 11. CMOS Logic Proposed Decrementer

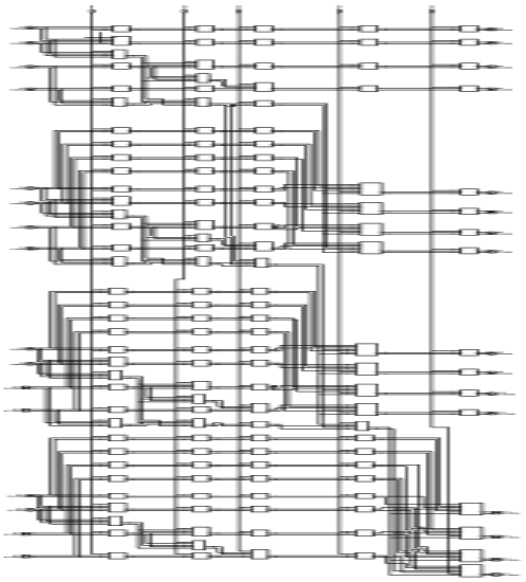

Figure 12. Adiabatic-Logic proposed Decrementer

TABLE III
POWER IN MILLIWATTS AT FREQUECIES IN MHZ FOR INCREMENTER

Circuit	Incrementer			
Frequency	50	200	300	500
Ripple-carry	0.655	2.6	5.19	7.76
Proposed CMOS	0.352	0.92	2.89	4.83
Adiabatic	0.038	0.36	0.927	1.68

TABLE IV
POWER IN MILLIWATTS AT FREQUECIES IN MHZ FOR DECREMENTER

Circuit	Decrementer			
Frequency	50	200	300	500
Ripple-carry	0.55	3.4	5.35	8.0
Proposed CMOS	0.32	2.4	4.25	6.0
Adiabatic	0.075	0.35	0.86	1.7

V. RESULTS AND DISCUSSIONS

To get the practical performance comparison made between the already circuits and the proposed incrementer decrementer circuits, the results obtained in the front end is tabulated in Table I. The proposed incrementer proves to be 25% faster than conventional one, while the decrementer is about 17 % faster. An area reduction of 8% of the proposed circuit from that of the conventional circuit has also been achieved in case of an incrementer and 6.2% in case of decrementer. Table III and IV present the power dissipation incurred by the three types of incrementer and decrementer circuits. The power presented is the average power component, while taking various combinations of the input signals at identified frequency values. This method helps us obtain a justifiable result.

The adiabatic incrementer realizes 17 times less power than the ripple-carry incrementer type at 50MHz. It realizes 4.62 times less power at 500MHz frequency of operation. The corresponding values of decrementer are 7.33 and 4.7 at 50MHz and 500MHz respectively.

The adiabatic power is the power incurred by the circuit, and it depicts the advantage of the adiabatic or energy recovery property of the circuit.

VI. CONCLUSION

A new circuit for the incrementer/decrementer is presented in this paper. The proposed circuit reduces the operation complexity and number of devices used. It paves way for reduced area, less power dissipation and lower energy added with increase in speed performance. The comparison results also show that the proposed adiabatic design reduces the circuit delay of a 16-bit incrementer by 25%, along with a power reduction from 0.55mW of the ripple-carry adder to 0.075mW of the adiabatic decrementer. The corresponding values of incrementer are reduction of adiabatic power from 0.655mW to 0.038mW at 50MHz. At 500MHz, power reduction from 7.76mW to 1.68mW of adiabatic circuit has been realized for the incrementer.

The decrementer realizes power reduction from 8.0mW to 1.7mW. The comparison pertaining the proposed CMOS incrementer circuit shows a power reduction of nearly 2 times at 50MHz to 1.6 times at 500MHz. The corresponding power reduction for decrementer is nearly 1.72 times at 50MHz to 1.33 times at 500MHz.

ACKNOWLEDGMENTS

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