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Signal Integrity modeling for high-speed DDRx Using Chip-Package Board analysis

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Abstract

Signal integrity (SI) is among the main concerns in the design process of high-speed printed circuit boards (PCBs). Under the platform of a double-data-rate memory module, a modeling method considering all the significant effects from the chip, package, and board levels is developed to identify and investigate the critical nets affecting the signal (SI). In SI part, accurate modelling strategies for signal channels are verified by experiments on samples of address lines. The analysis indicates that the parasitic effects of the low-cost package structure are the most critical, depicting the importance of improved package design. It propose, investigate the system bottleneck for the current design of a DDR3 memory module, reducing Crosstalk Noise, Reflection Noise, Power/Ground Noise and electromagnetic interference of SI and board design, layout for sigxplorer. The analysis indicates that the parasitic effects of the low-cost package structure are the most critical, depicting the importance of improved package design in the next-generation DDR.

Keywords*- signal integrity (SI), Double-data-rate synchronous dynamic RAM(DDR SDRAM), model extraction.*

1. INTRODUCTION

Signal Integrity (SI) is the practice of ensuring sufficient fidelity of a signal transmitted between a driver and a receiver for proper functioning of the circuit, e.g., the signals over the high-speed bus between a processor and its chipset. Owing to the benefits of low cost and high quality, the double-data-rate synchronous dynamic RAMs(DDR SDRAMs) are currently being developed for today's high-endcomputers and workstation applications.. The term Signal Integrity (SI) addresses two concerns in the electrical design aspects , the timing and the quality of the signal. The goal of signal integrity analysis is to ensure reliable high-speed data transmission

Table i
evolution of DDR SDRAM

Specification	DDR1	DDR2	DDR3	DDR4
Operating Voltage (V)	2.5	1.8	1.5	1.2
Data-rate (Mbps)	200/266/ 333/400	400/533/ 667/800	800/1066/ 1333/1600	1600/2133/ 2667/3200
Setup + Hold Time (ps)	900	500	305	125

It can be seen that the operating voltage is lower with increasing data rates, high performance and lower power consumption. non ideal effects, such as crosstalk noise [1]–[2], reflection noise [3], and simultaneous switching noise (SSN) [4], previously regarded as negligible have become major design challenges for satisfying the requirements of signal integrity (SI) inside the package and board levels. This paper focuses on the modeling of the SI issues for different kinds of signal groups, i.e., command lines, address lines, clock lines, and data buses, under the platform of a high-speed DDR memory system.

2. MEMORY MODULE OVERVIEW

"Double Data Rate", DDR technology doubles the bandwidth of SDRAM under optimal conditions. This is to say that twice as much data can be transferred between the memory and system during the same amount of time. SDRAM transfers data on every clock cycle (to be specific, on the rising edge of every clock cycle), while DDR transfers data on both the rising edge (clock signal bounces from LOW to HIGH) and the falling edge (clock signal bounces from HIGH to LOW) of a clock cycle.The DDR3 memory module, also named as dual in-line memory module, is denoted in Fig. 1(a) All signal groups, except the data buses, implement the flyby topology , which sweeps long distances from the left side of PCB to the right. Fig. 1(b) shows the cross section of the memory module. From Fig.1(a) there are eight units of SDRAM and each of the units is composed of a memory chip with the associated package substrate. The memory ICs are directly connected to the package with bond wires, and printed circuit board (PCB) are linked by solder balls. The package is surface mounted on the memory module board (PCB) with the BGA typed interconnects. The whole signal interconnects and the corresponding PDNs inside the DDR3 memory module can be divided into three groups, include the clock lines, the command/address lines, and the data buses[6].

The PCB is a 6 layer FR4 boards with complicated power/ground traces and planes. The extraction methods for the equivalent models of the PDS at three different levels are described in the following. The accuracy of the constructed models is also verified. Several methodologies have been reported for modeling of power/ground plane noise. Three-dimensional full-wave approaches include the method of moments (MoM) with integral equations , the partial element equivalent circuit (PEEC)method with retardation effects, and

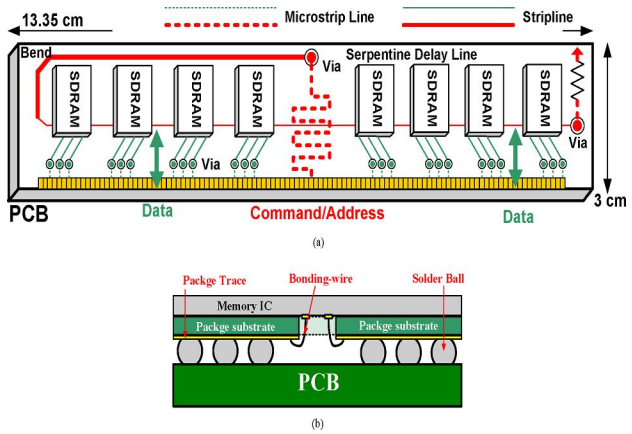

Figure.1. Physical structure of DDR SDRAM memory module. (a) Top view. (b) Cross-sectional view

the finite-difference time-domain method (FDTD) with broadband responses in one simulation [5].Planes for power and ground levels are commonly used for the PDN in multilayer packages or PCBs .For long high speed interconnects, differential lines are widely used because of their immunity to noise, crosstalk, and electromagnetic interference.

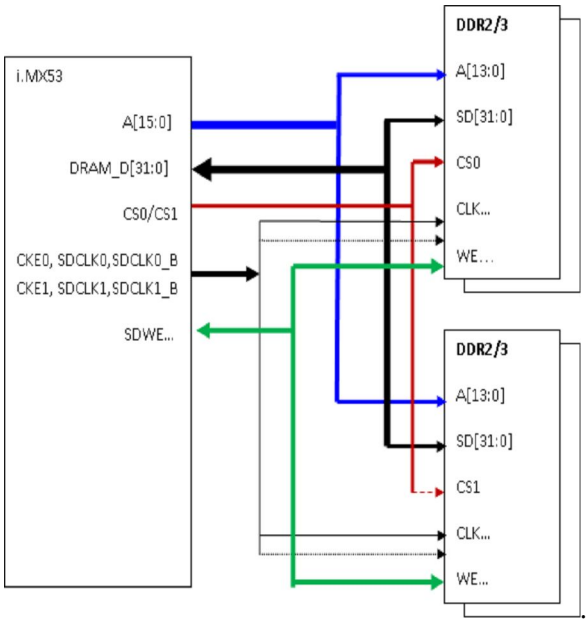

Figure.2. Interfacing of I.MX.53X with DDR3 memory

From fig.2 The DDR3, 1 GBit memory is interfacing with i.mx53x processor. The memory has the capability of 32-bit data, 14-bit Address & External clock source from processor. In application micron MT1213hj2h323 as interfacing for industrial and commercial purposes with various applications. The DDR3 memory as operated low voltage of 1.5V.

To increase memory capacity and bandwidth, chips are combined on a module. For instance, the 64-bit data bus for DIMM requires eight 8-bit chips, addressed in parallel. Multiple chips with the common address lines are called a memory rank. The term was introduced to avoid confusion with chip internal rows and banks. A memory module may bear more than one rank.A test sample comprised of a ball grid array (BGA) package mounted on a PCB was fabricated. off-chip drivers (OCDs) need to have a rapid current transient at their outputs. The data buses suffer from severe SSNs due to the connected OCDs with swift voltage transient. the effects of connection in parallel have no influence on the input impedance of complete PDS at low frequency.As the signal traces of data buses on the PCB are much shorter; the SI problems of the data buses are not serious.

3. SI ANALYSIS IN I.MX53X

The MCIMX53xA (i.MX53xA) automotive infotainment processor is Freescale Semiconductor's latest addition to a growing family of multimedia-focused products offering high performance processing with a high degree of functional integration aimed at the growing automotive infotainment, telematics, HMI, and display-based cluster markets. This device includes 3D and 2D graphics processors, 1080i/p video processing, and dual display, and provides a variety of interfaces.

The i.MX53xA processor features Freescale's advanced implementation of the ARM™ core, which operates at clock speeds as high as 800 MHz and interfaces with DR2/LVDDR2-800, LPDDR2-800, or DDR3-800 DRAM memories. This device is well suited for graphics rendering for HMI, navigation, high performance speech processing with large databases, video processing and display, audio playback, and many other applications. The flexibility of the i.MX53xA architecture allows for its use in a wide variety of applications. As the heart of the application chipset, the i.MX53xA processor provides all the interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, camera sensors, and dual displays.

Freescale delivers the ultimate in performance and design flexibility with its Smart Application Blueprint for Rapid Engineering (SABRE) platform for automotive infotainment based on the i.MX53 family of automotive applications processors. A high-performance, market-focused development system, the SABRE platform for automotive infotainment offers a solid foundation for next-generation converged telematics and infotainment platform designs.

The i.MX53 family of automotive applications processors represents Freescale's next generation of advanced multimedia and power-efficient implementation of the ARM® Cortex™-A8 core for the automotive market. With core processing speeds up to 1 GHz as well as a high-level integration, the SABRE platform for automotive infotainment enables customers to re-create today's consumer user experiences in the car. In analog circuits, designers are also concerned with noise that arise from physical sources, such as thermal noise, flicker noise,and shot noise. These noise sources on the one hand present a lower limit to the smallest signal that can be amplified, and on the other, define an upper limit to the useful amplification.In digital ICs, noise in a signal of interest arises primarily from Increasing interconnect density has led to

each wire having neighbors that are physically closer together, leading to increased coupling capacitance between neighboring nets. As circuits have continued to shrink in accordance with Moore's law, several effects have conspired to make noise problems worse. IBIS specifies a consistent software-parsable format for essential behavioral information. With IBIS, simulation tool vendors can accurately model compatible buffers in SI simulations.

4. SIGNAL NET TO BE PERFORMING SI ANALYSIS

The SI Analysis carried out for Data, Address and Control signals. Those signal groups as listed below:

The memories have 32 bit Data & 14 bit Address, so data are to grouping with 4 byte. This byte has 8 bit data for each byte. The DQS is strobe, when strobe signal is to be enabling that time only memory can write the data with one signal DM0 is data mask for each bye. In address group the signals of Bank Address with Selection (RAS, CAS) as applied. The Data & Address group for bus simulation as given below table.

Table.2 Bus Grouping For Signal Net

S .No	Bus Name	Signals
1	Data Byte_1	EMI_D00-D07 EMI_DQS0/0B EMI_DM0
2	Data Byte_2	EMI_D08-D15 EMI_DQS1/1B EMI_DM1
3	Addr ess	EMI_A0-A14 EMI_BA0/BA1/BA2 EMI_CLK0/0B EMI_BA0/BA1/BA2 EMI_CLK0/0B

Models for Processor (U1)

The IBIS model of i.mx287 as downloaded from Freescale and corresponding DDR2 package as assigned to them. IMX287→i_MX28_14X14_IBIS_v1p2.ibs

Model for Memory (U2)

The IBIS model of MT47H64M16HRas downloaded from Micron and corresponding DDR2 package as assigned to them.

DM→MT47H64M16HR, V69A-DM-INPUT-400/533
DQ→MT47H64M16HR, V69A-DQ-400/533
DQS→MT47H64M16HR, V69A-DQS-400/533

5. RESULT ANALYSIS

The Simulation results carried out for Reflection & Crosstalk for DDR3 with various strategies.

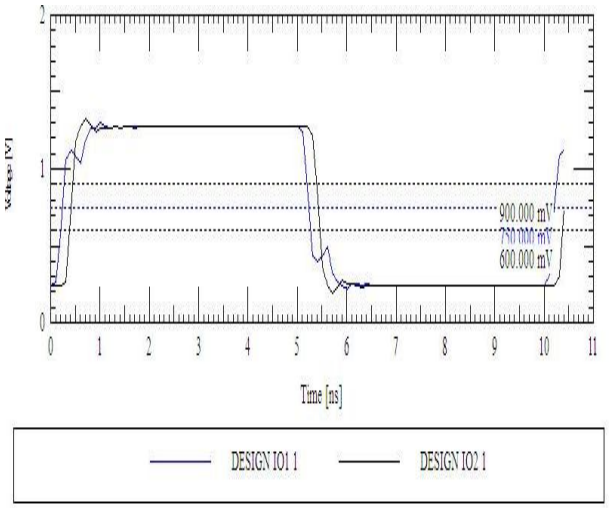

Figure. 3Simulation waveform for DDR3 with 1.5V, 1600 MHz for reflection.

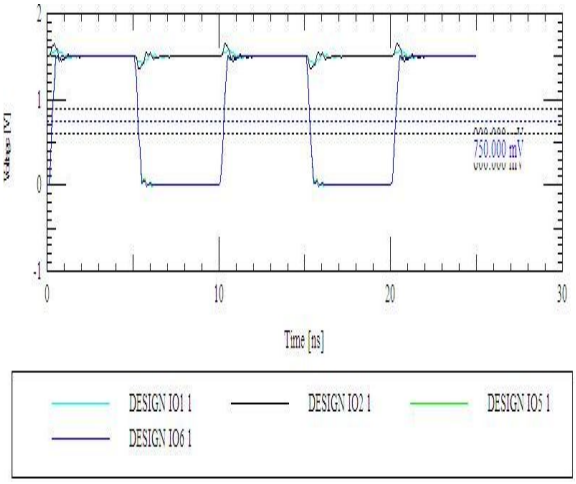

Figure. 4 Simulation Waveform for DDR3 with1.5V, 1333MHz for Crosstalk

Fig4 shows Simulation Waveform for DDR3 with1.5V, 1333MHz for Crosstalk .The PDN from the transistor level to the system level can be mainly described by three kinds of elements, shunt capacitors, series inductors, and distributed transmission lines[9].

The insertion & return losses are calculated for the transmission line for the data & Address Signals. The insertion loss & return loss are calculated at 205 MHz operating frequnecy.

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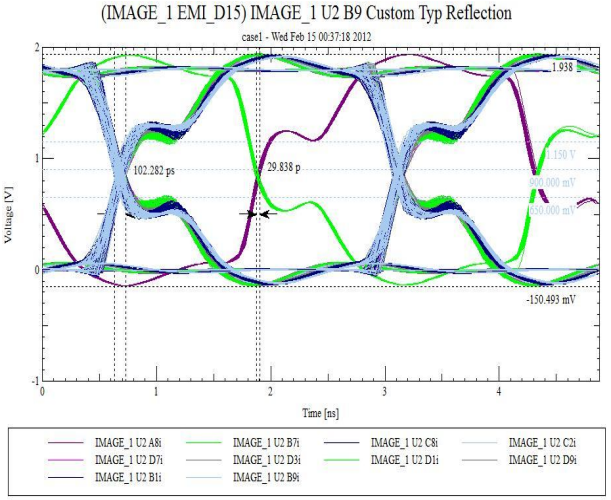

Figure. 5 Eye Diagram For Data_Byte_2 During write Cycle With (A) 150 Ohm ODT

The Eye Diagram can be obtained by 256 bits of signals are transmitted for both data & address. The Eye Diagram Analysis used to determine the Setup & Hold Timing for I.MX287

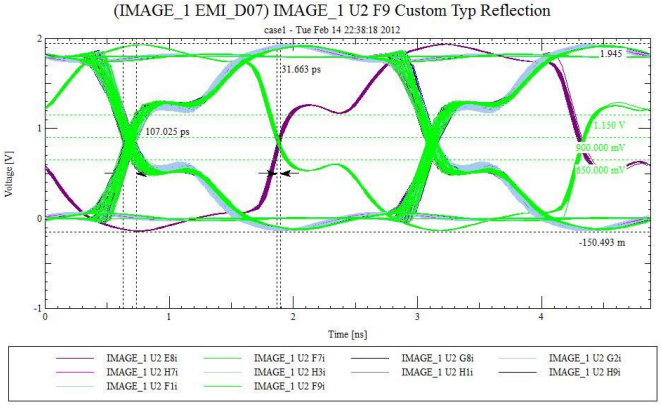

Figure. 6 Eye Diagram For Data_Byte_1 During write Cycle With 150 Ohms ODT

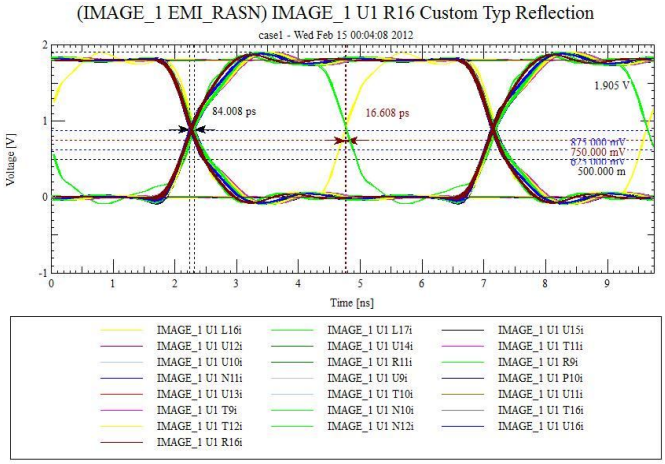

Figure. 7 Eye Diagram for Address signals

6. CONCLUSION

An analysis methodology is proposed to investigate the system bottleneck for the current design of a DDR3 memory module. For the SI part, the characteristics of three major signal categories are clearly clarified to understand their difficult points. After that, complete modeling methods for the signal traces are discussed, and the modeling accuracy has been verified up to 10 GHz by measurements on samples of address. The SI is also investigated both in the time and frequency domains.In addition, it will become increasingly critical to code sign SI, and EMC, in order to achieve the design objectives of high quality, low emission, cost reduction, as well as reduced time.

For the command/address lines, SI problems play a very important role. For the present case, the time-domain simulation shows that the eye quality is improved by 35.2% with the thin trace compensation .

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